

Fig. 1

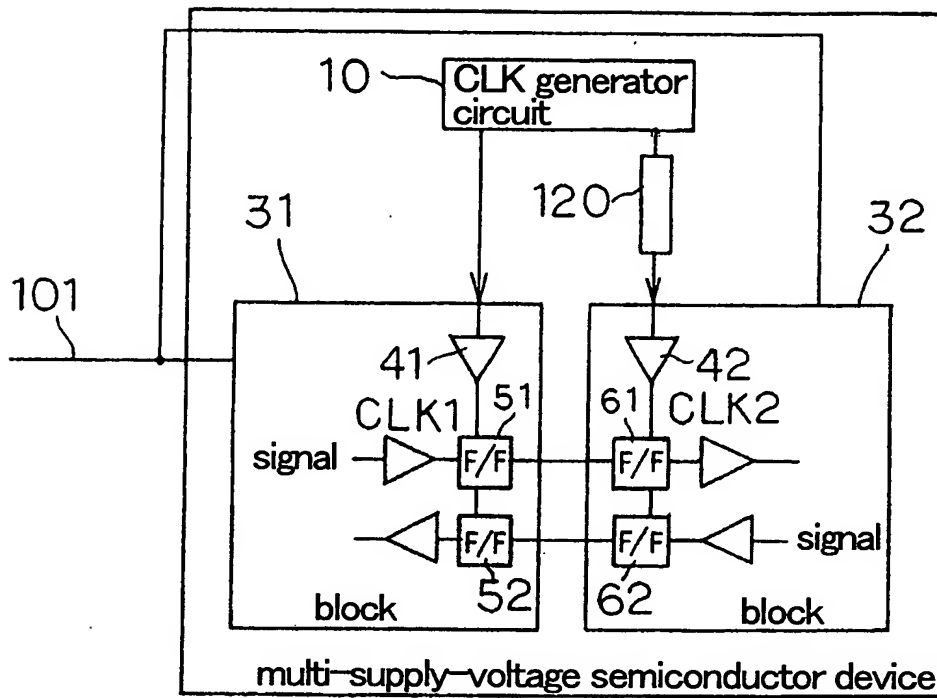


Fig. 2

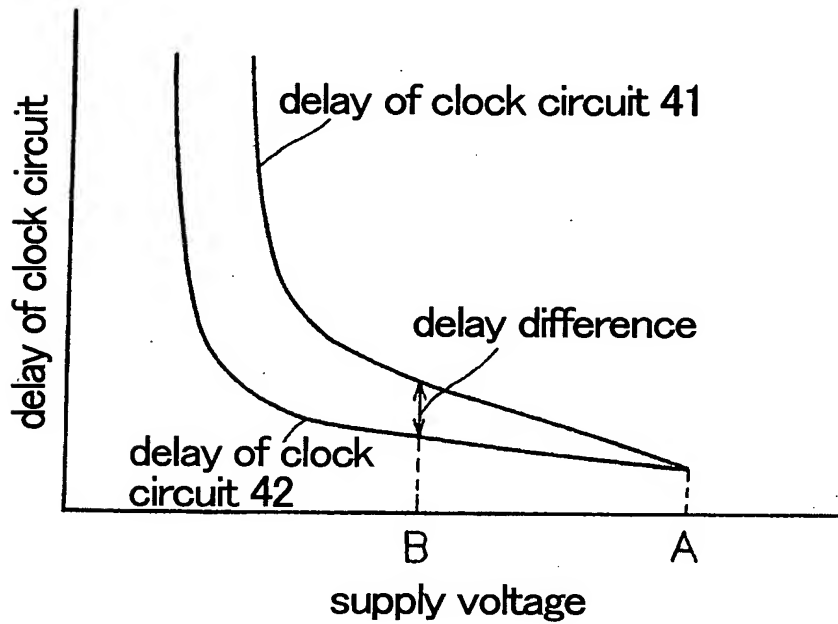


Fig. 3

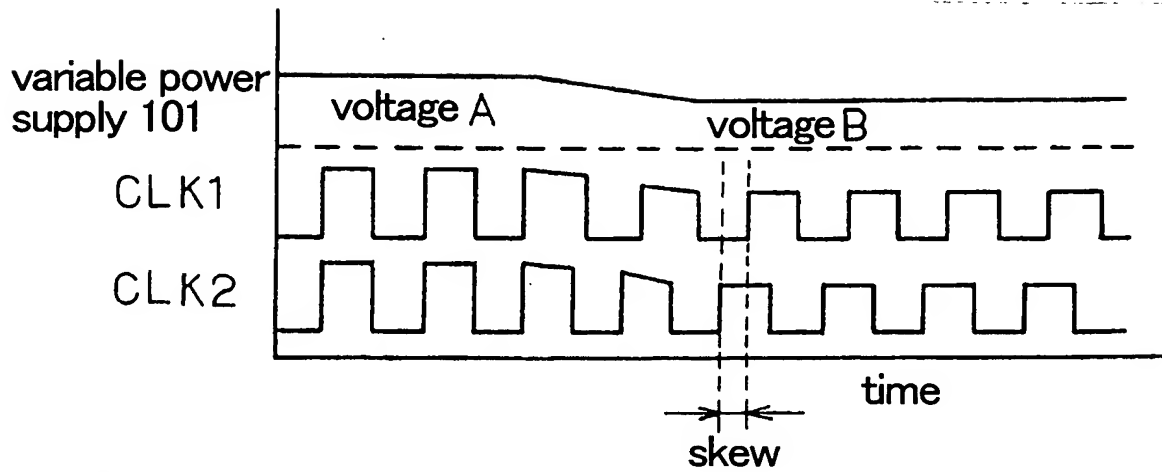


Fig. 4

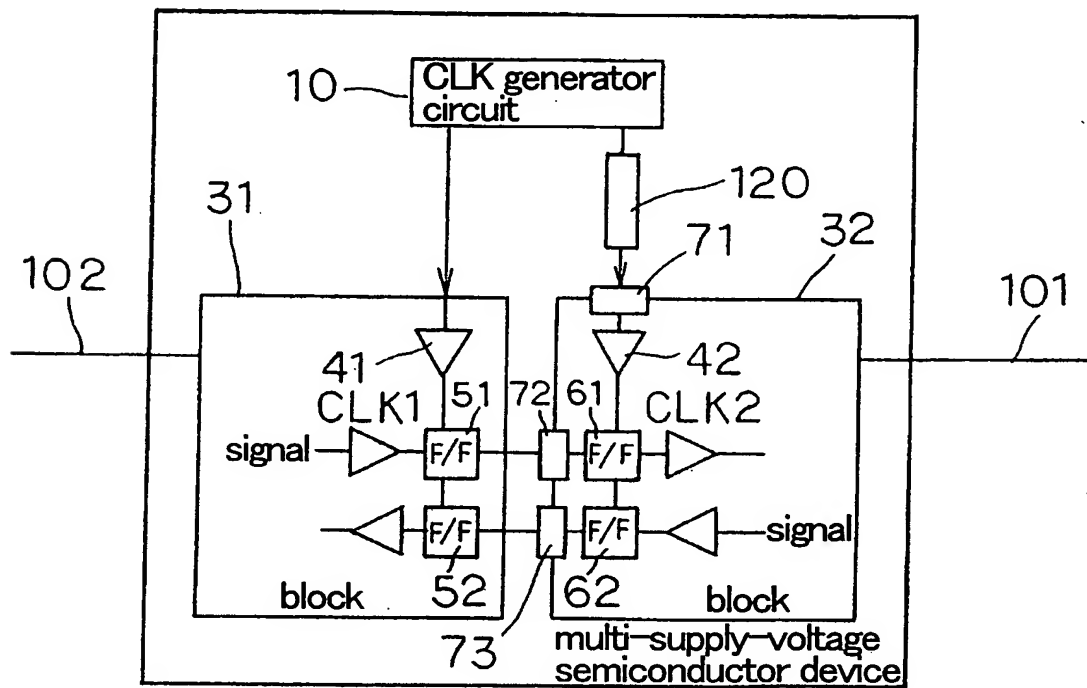


Fig. 5

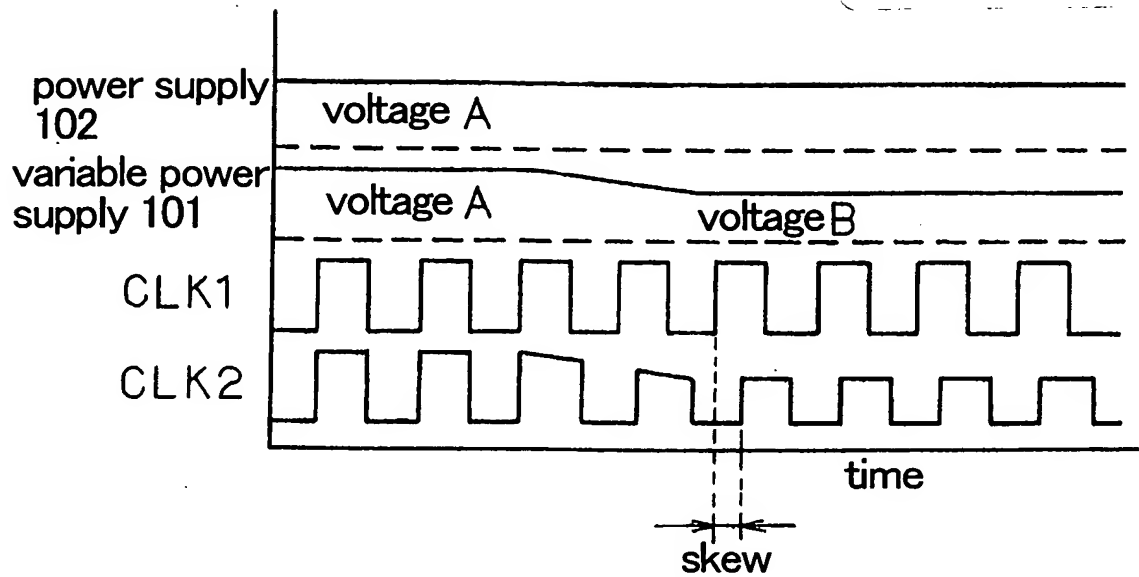


Fig. 6

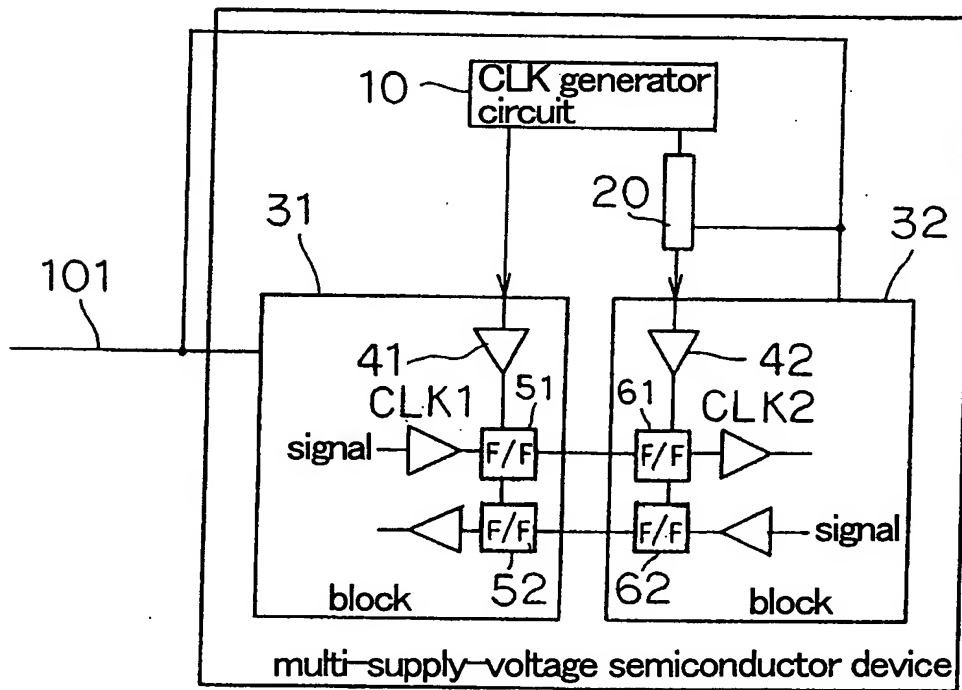


Fig. 7

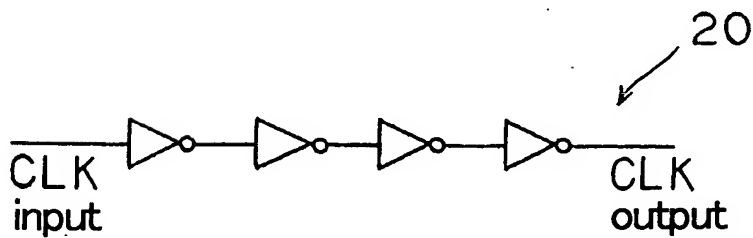


Fig. 8

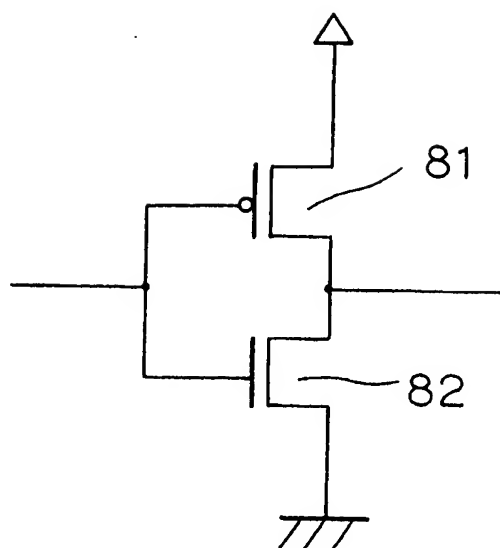


Fig. 9

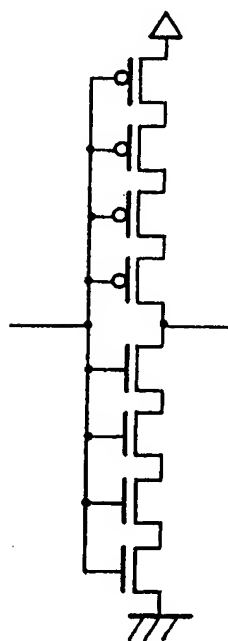


Fig. 10

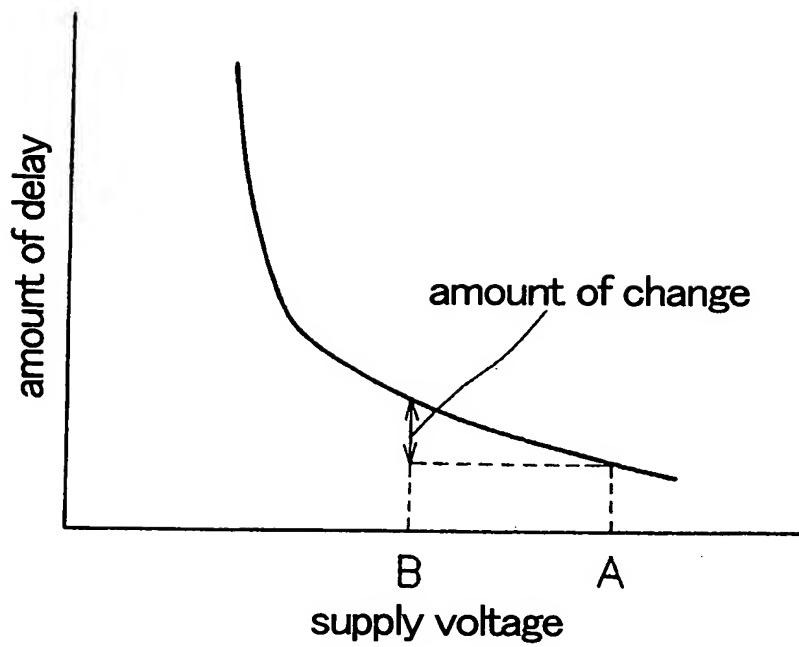


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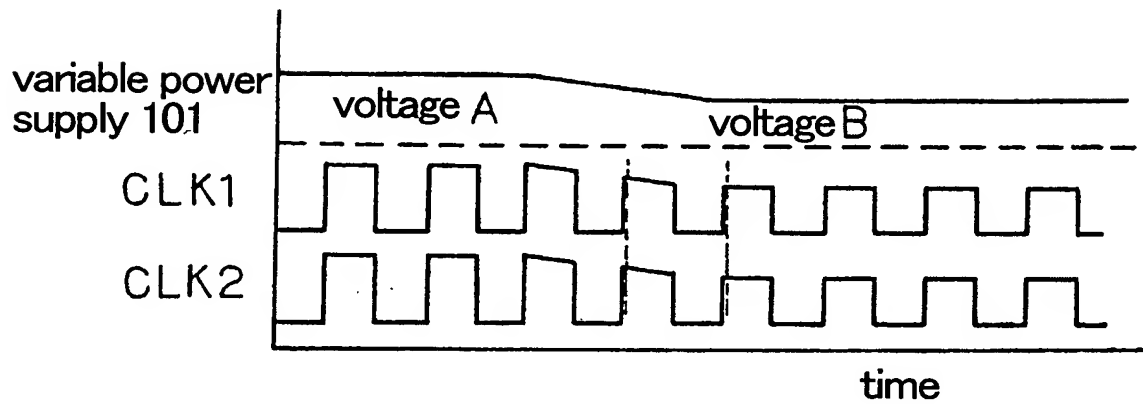


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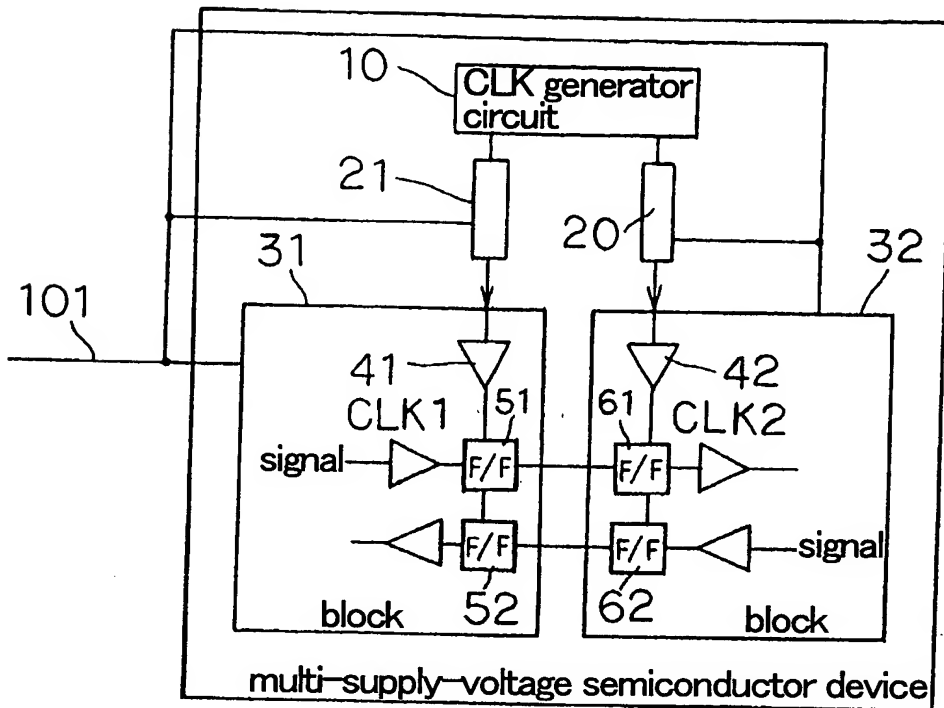


Fig. 13

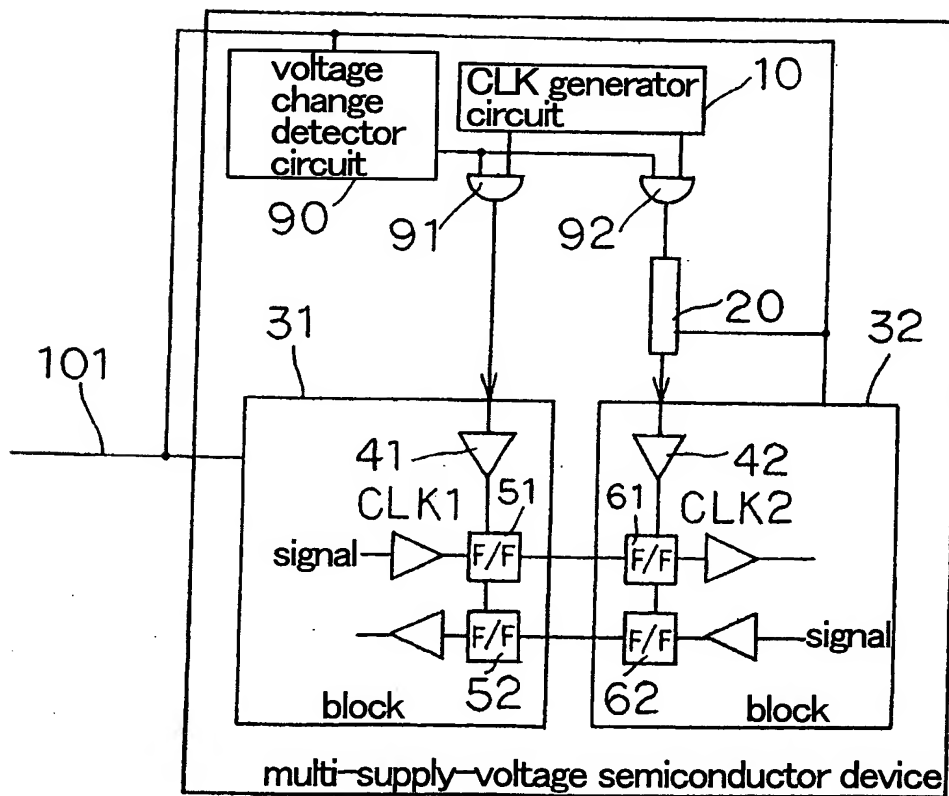


Fig. 14

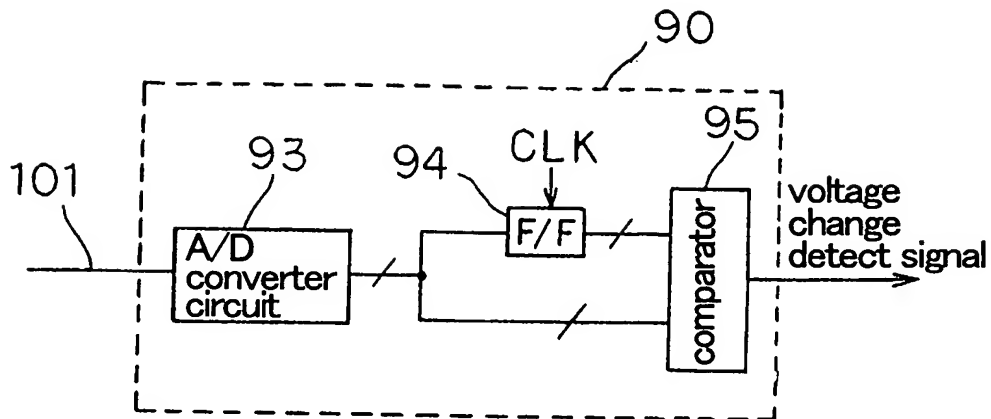


Fig. 15

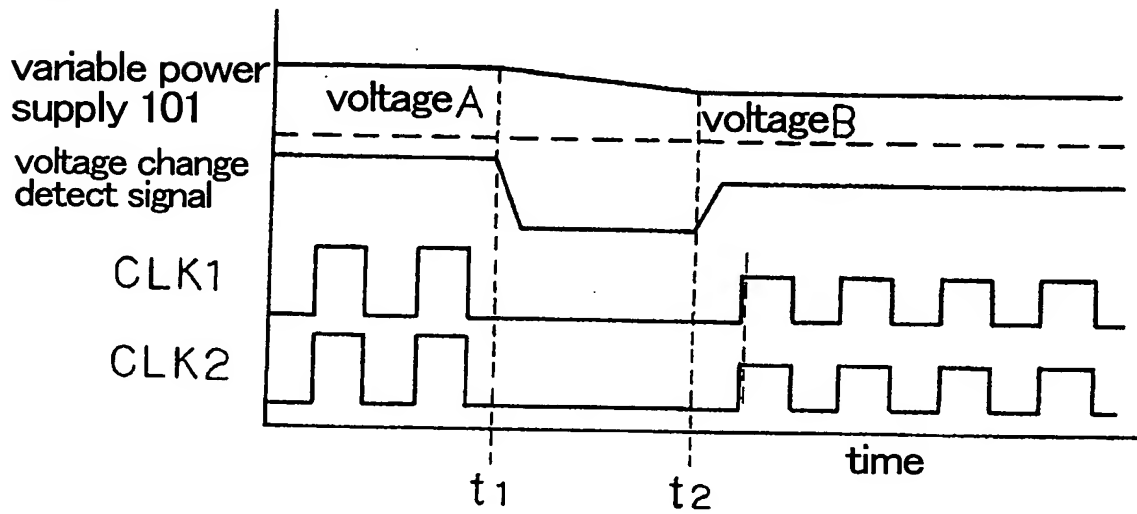


Fig. 16

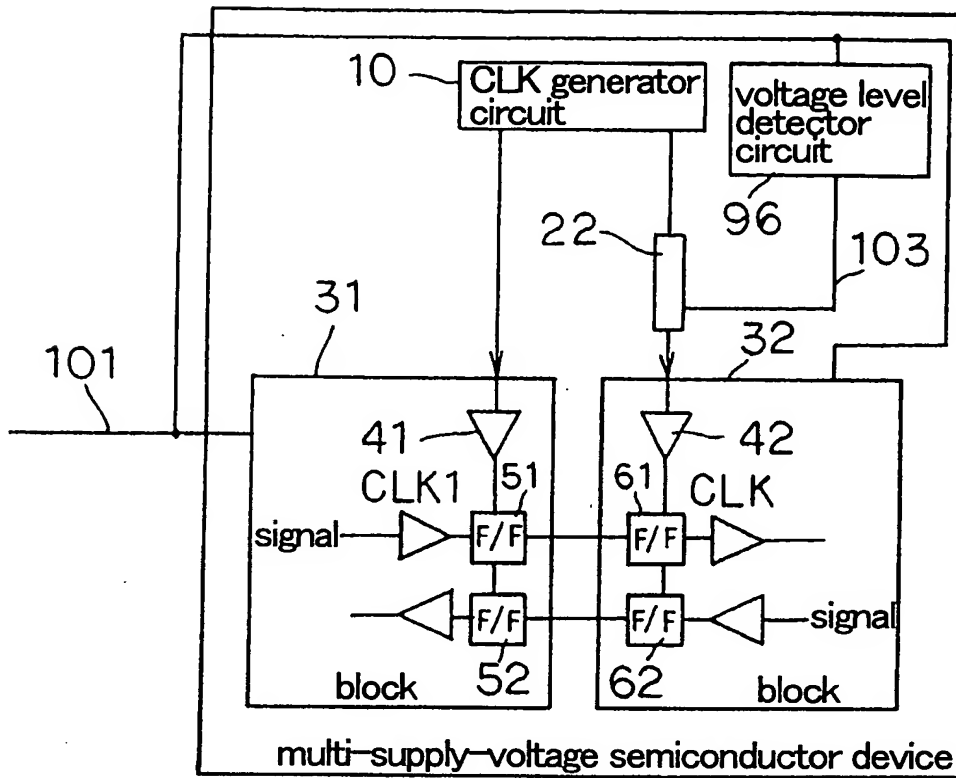


Fig. 17

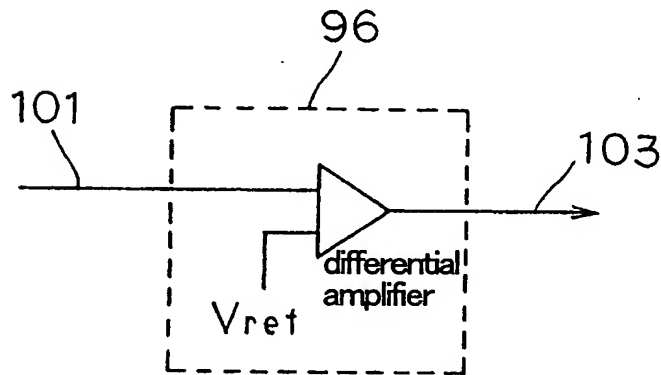


Fig. 18

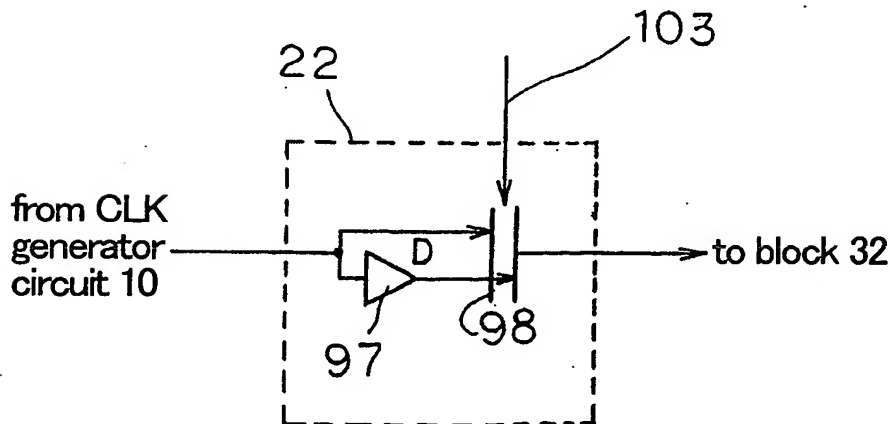




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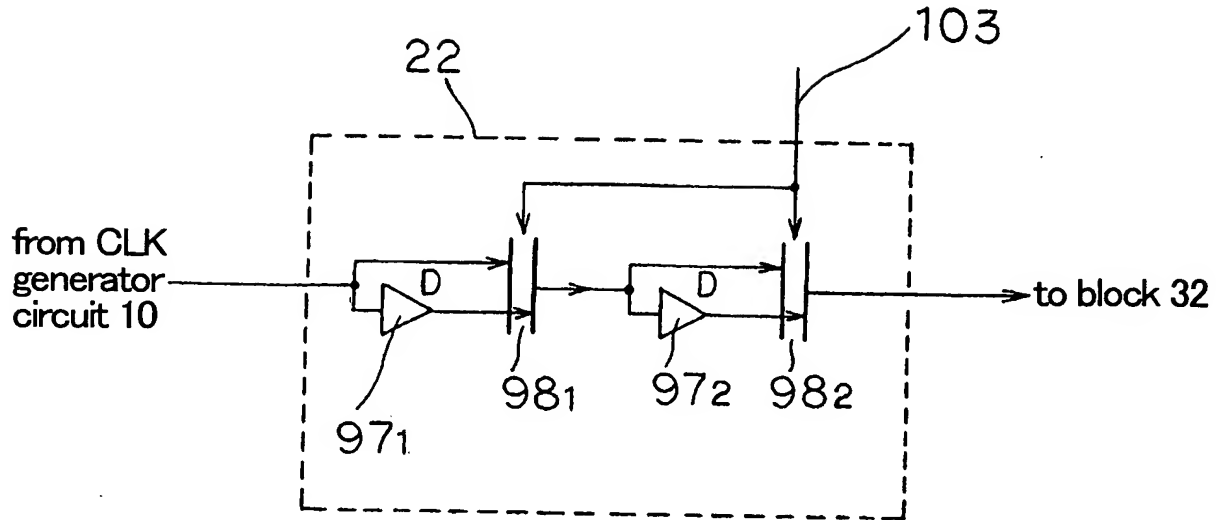


Fig. 20

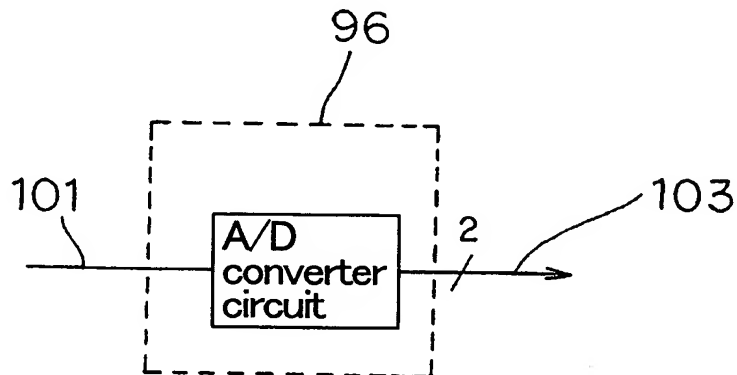
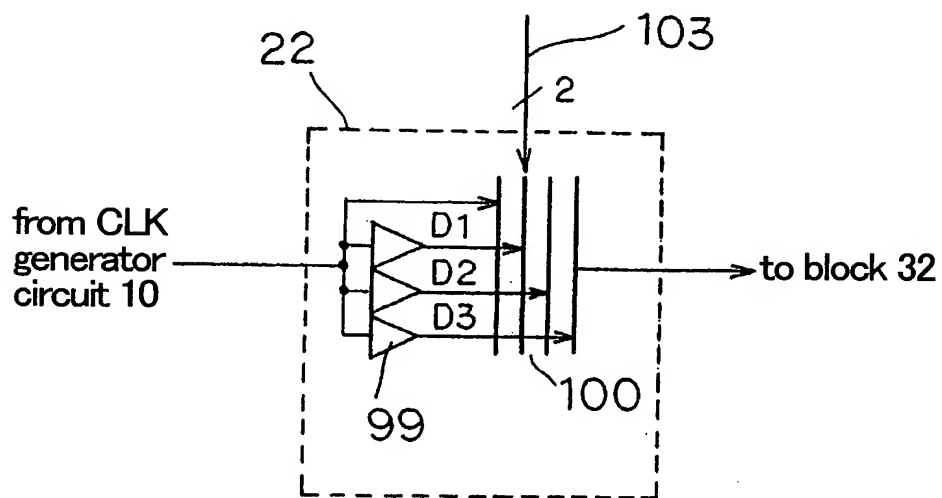


Fig. 21



multi-supply-voltage semiconductor device

The diagram illustrates the timing of a power supply regulation system. It features five horizontal axes representing different signals over time:

- variable power supply 101:** Shows a voltage ramp down from **voltageA** to **voltageB**. A dashed horizontal line indicates a reference level.
- voltage change detect signal:** A signal that transitions from high to low at time  $t_1$  and back to high at time  $t_2$ .
- voltage level detect signal 103:** A signal that transitions from **level A** to **level B** at time  $t_1$  and back to **level A** at time  $t_2$ .
- CLK1:** A square wave clock signal that is active during the initial ramp down and again after time  $t_2$ .
- CLK2:** A square wave clock signal that is active during the initial ramp down and remains active after time  $t_2$ .

Vertical dashed lines mark the times  $t_1$  and  $t_2$ , which correspond to the points where the power supply voltage changes and the detect signals transition.

multi-supply-voltage semiconductor device

Fig. 26

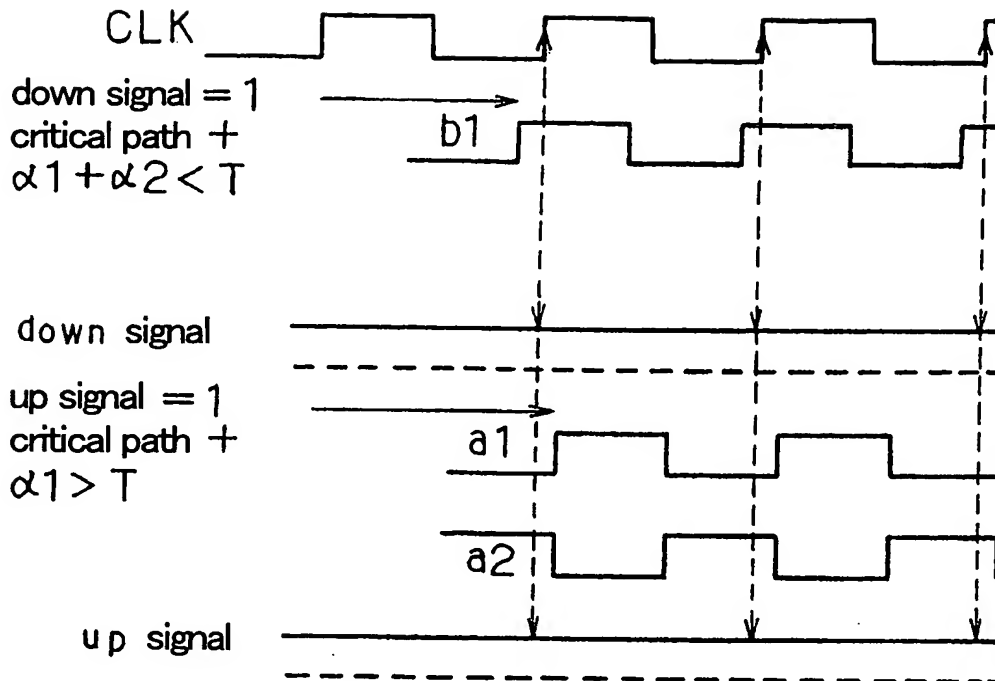


Fig. 27

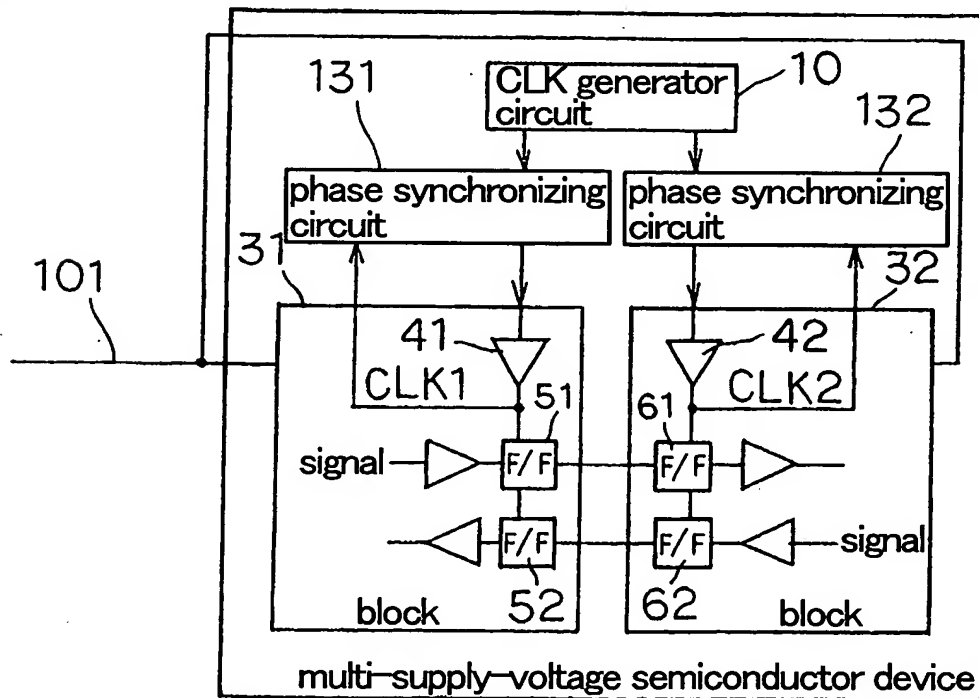
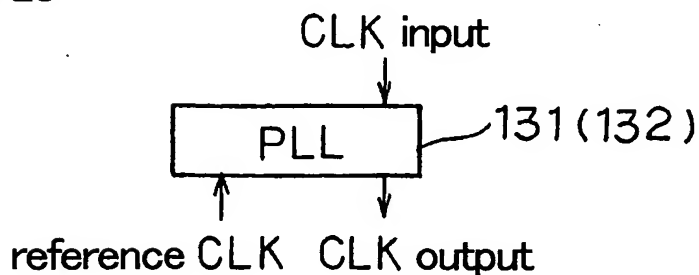


Fig. 28



A block diagram of a DLL (131). The block is a rectangle labeled "DLL". It has three external connections: a "CLK input" at the top with a downward arrow, a "reference CLK" at the bottom left with an upward arrow, and a "CLK output" at the bottom right with a downward arrow. A reference numeral "131 (132)" is connected to the right side of the block.

variable power supply 101

voltage A

voltage B

CLK1

CLK2

time

multi-supply-voltage semiconductor device

Fig. 32

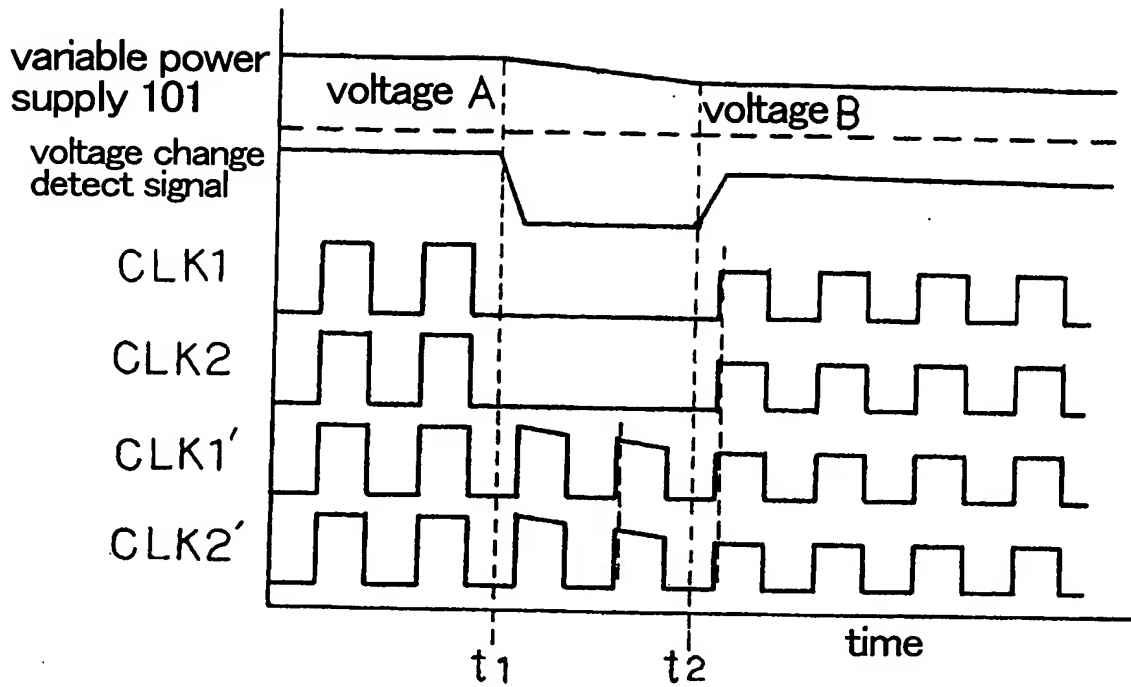


Fig. 33

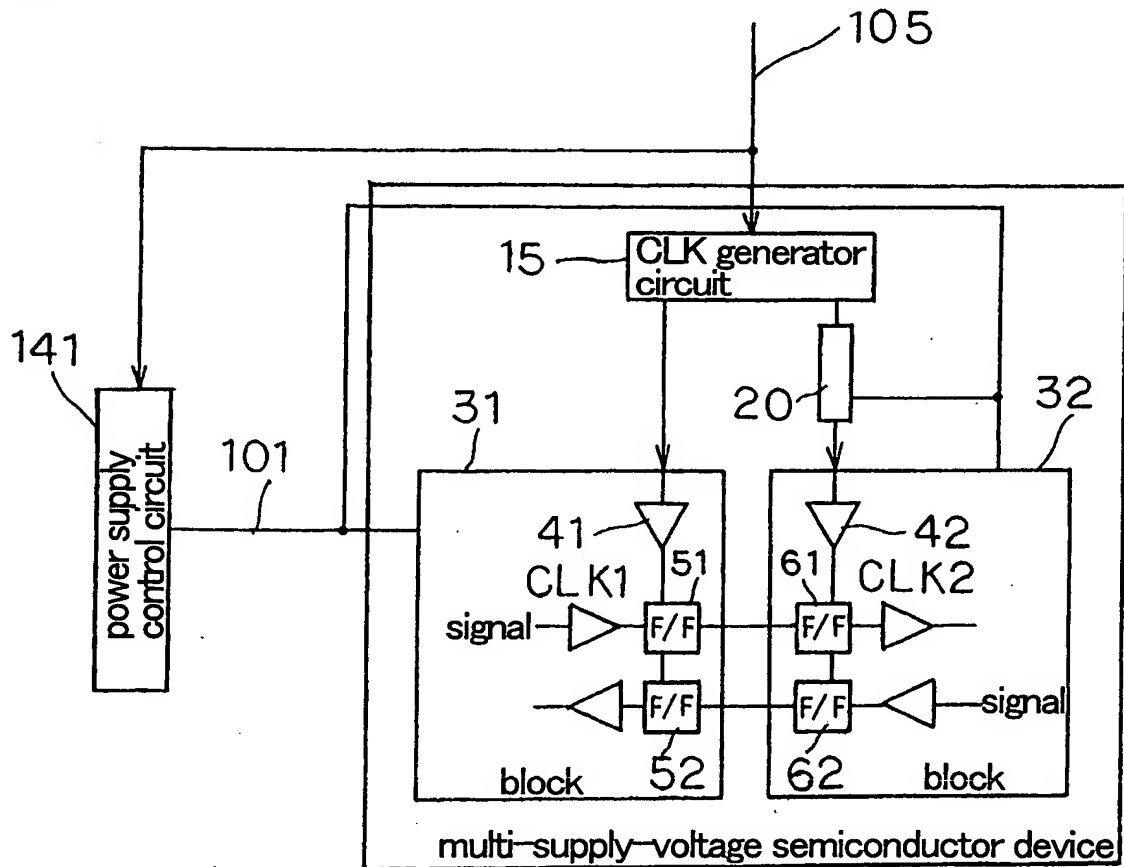


Fig. 34

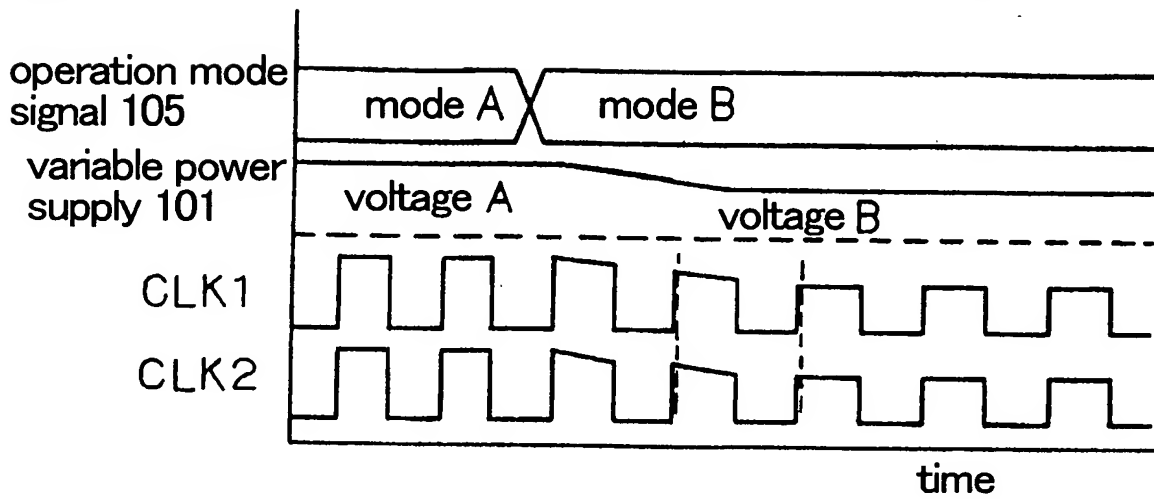


Fig. 35

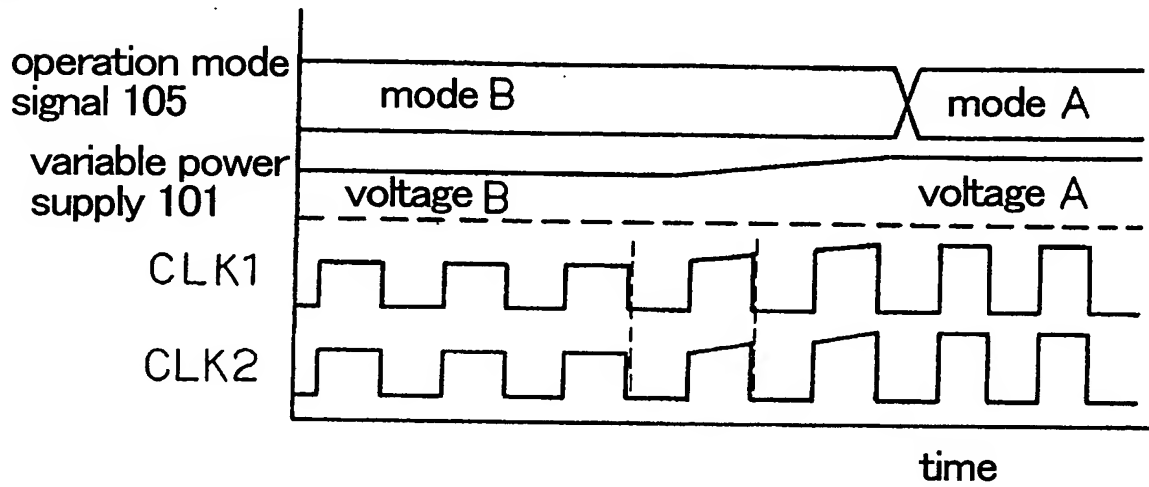


Fig. 36

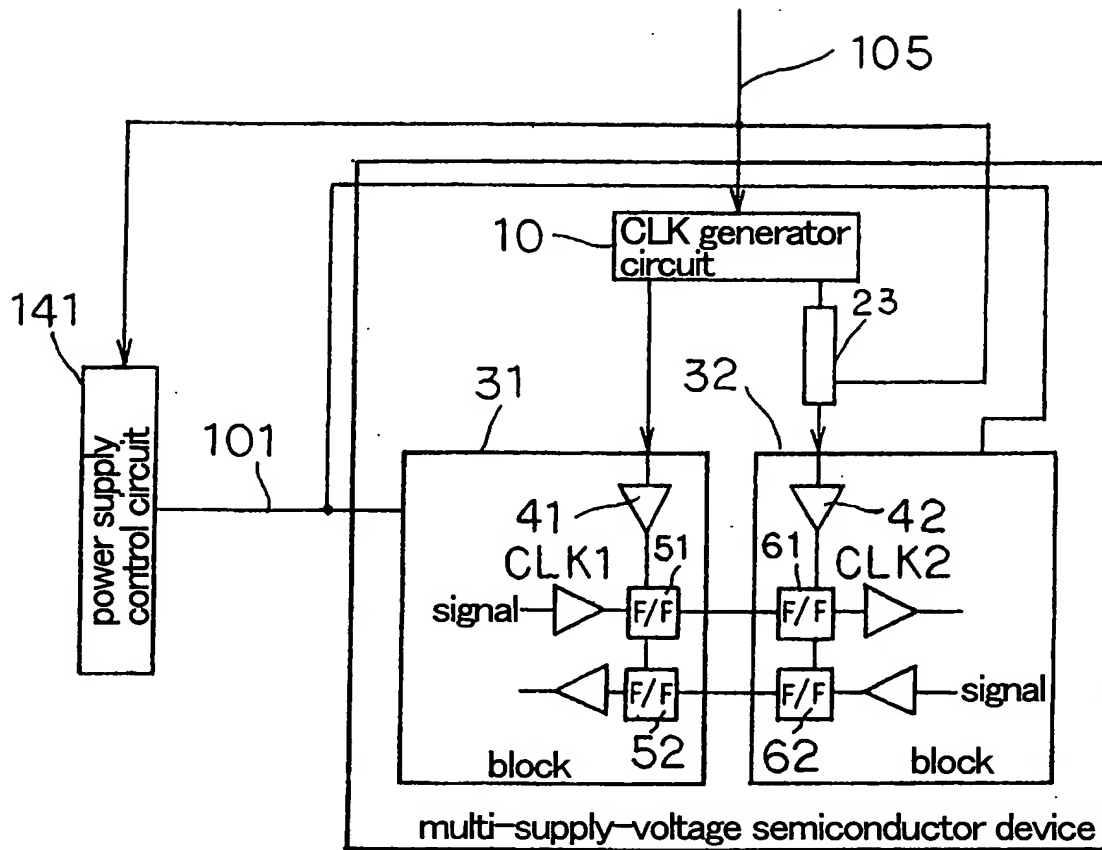




Fig. 37

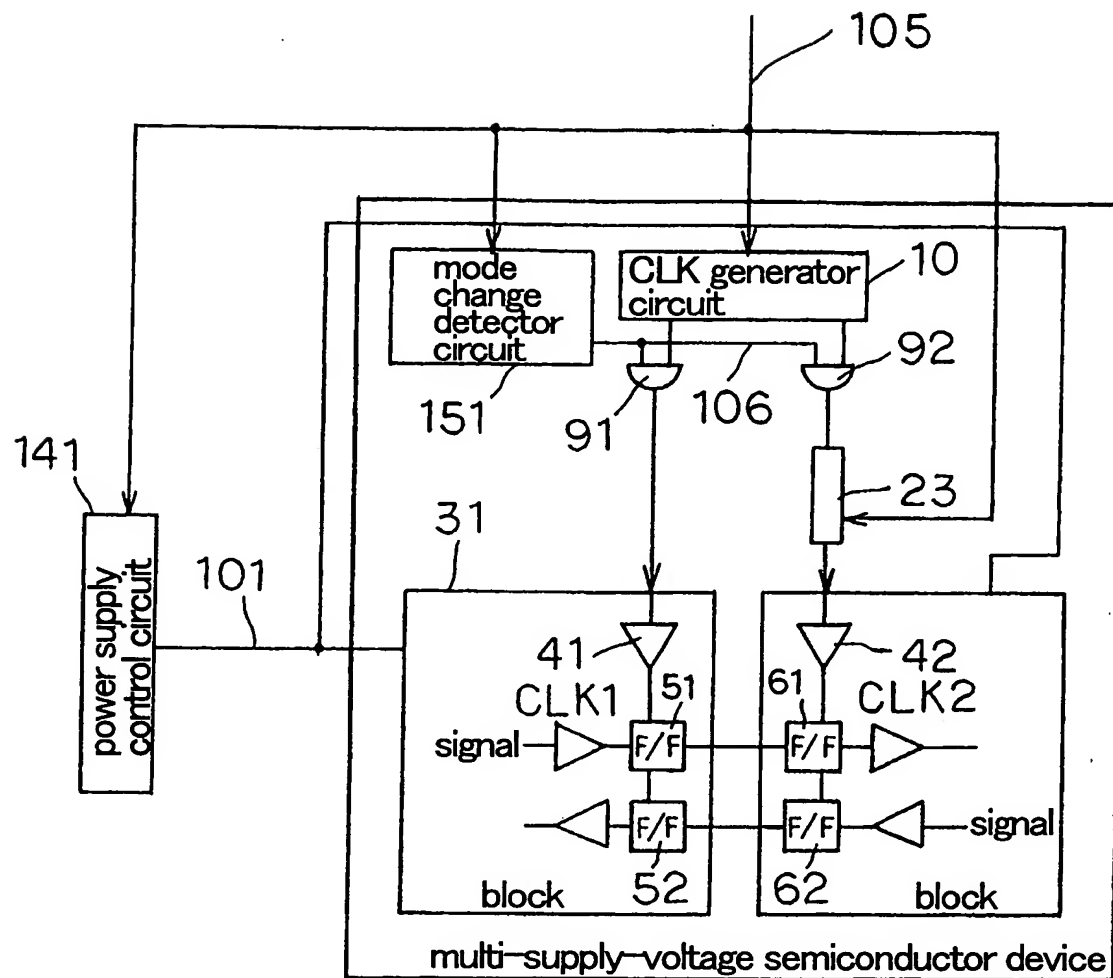


Fig. 38

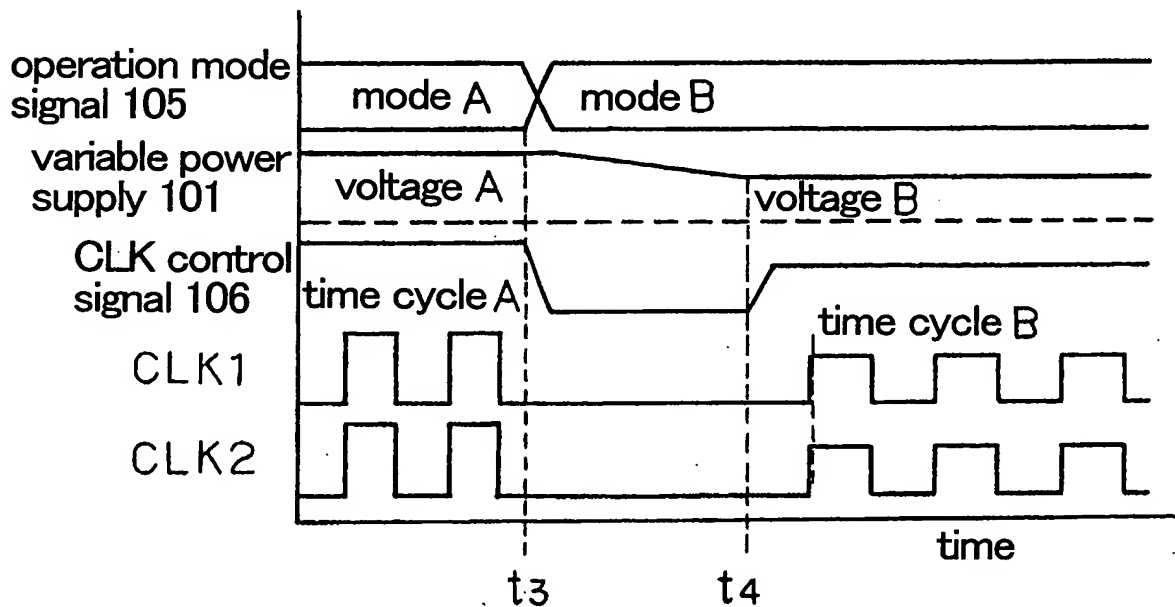


Fig. 39

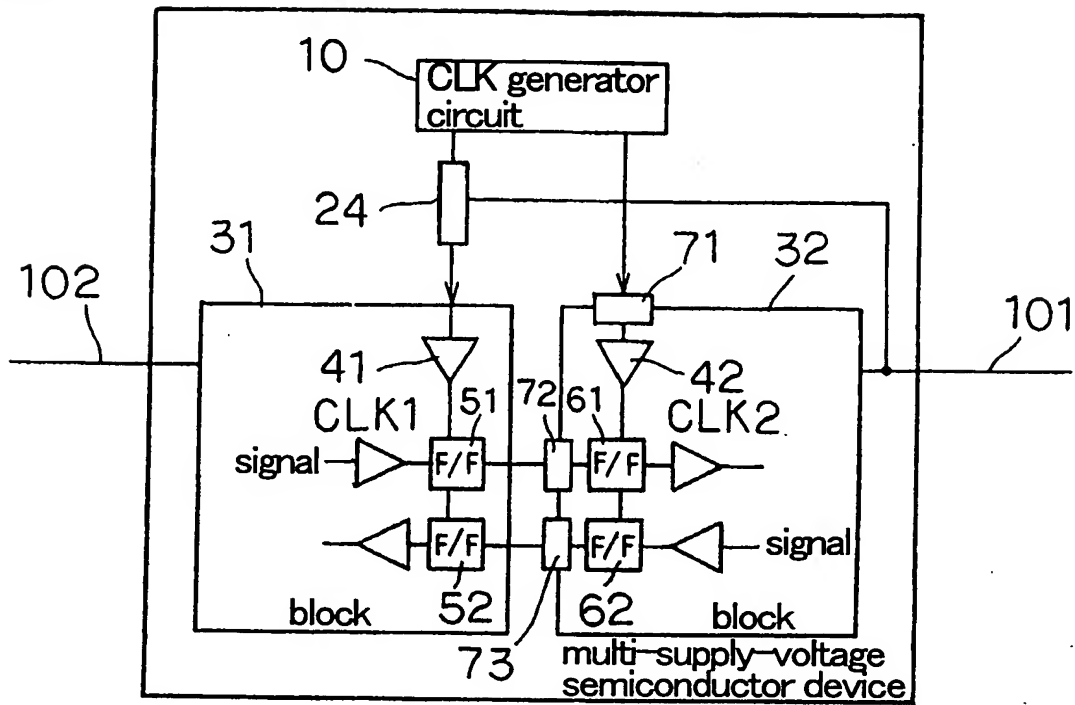


Fig. 40

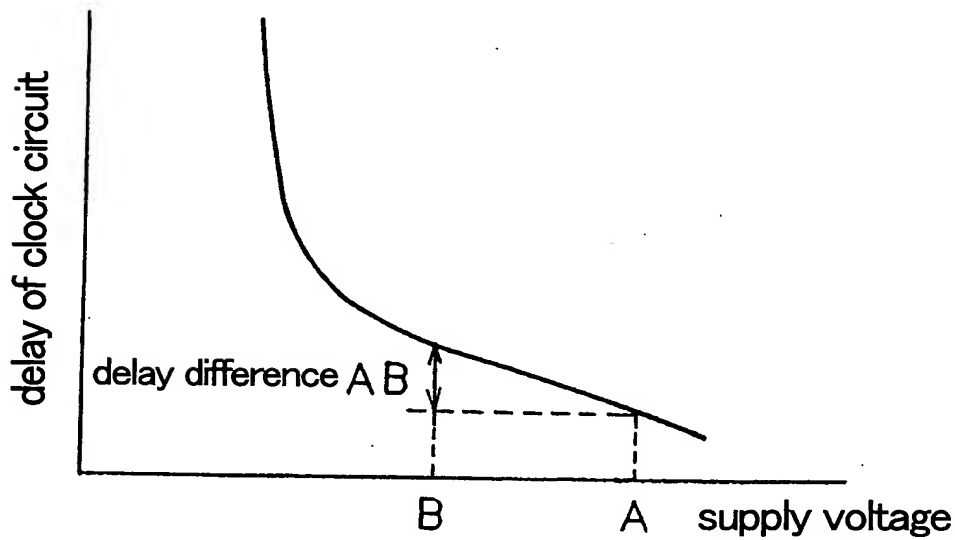


Fig. 41

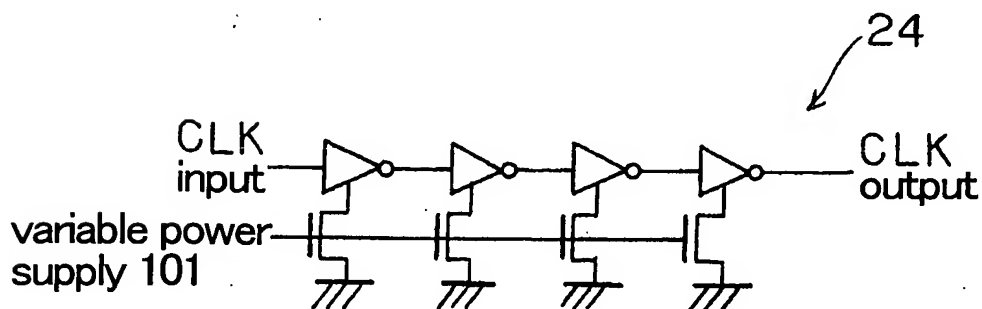


Fig. 42

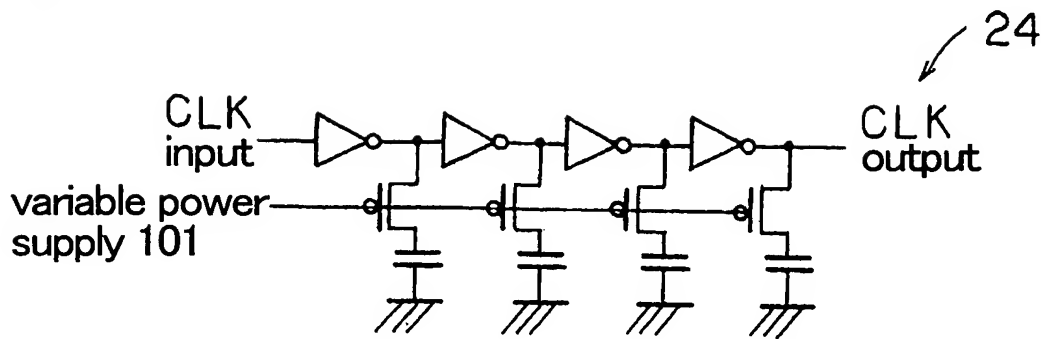


Fig. 43

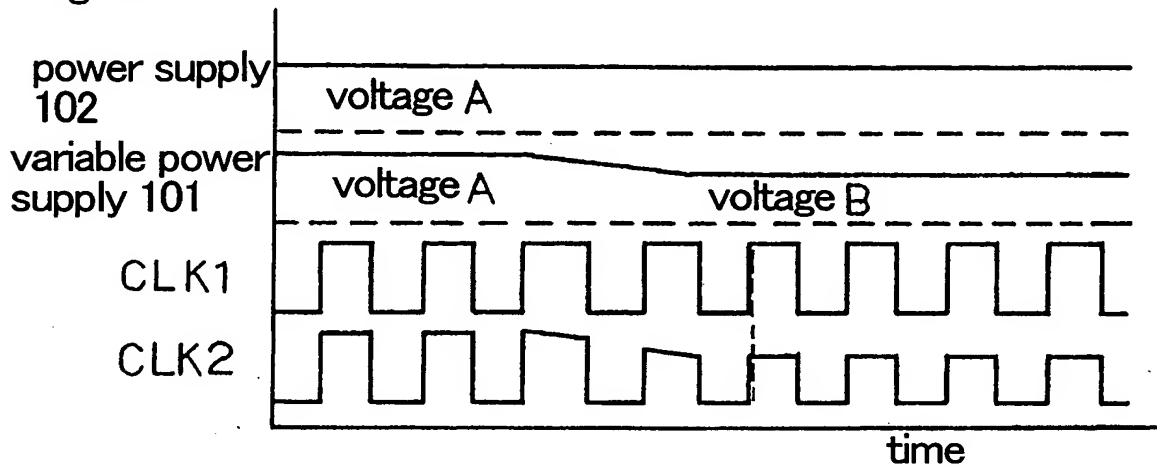


Fig. 44

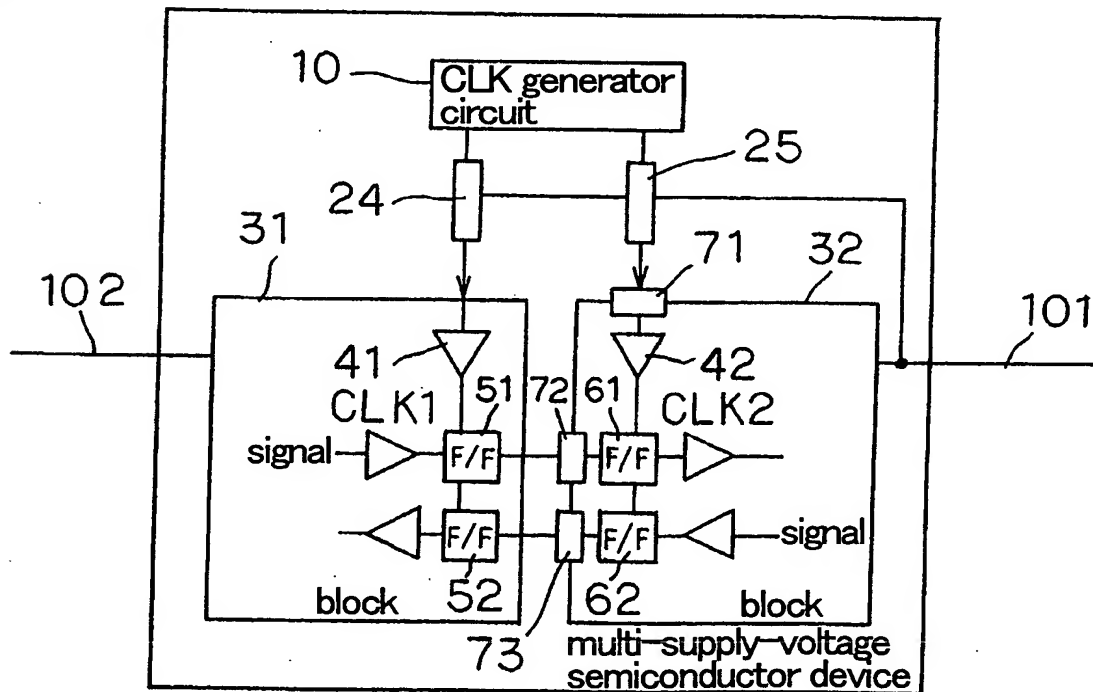


Fig. 45

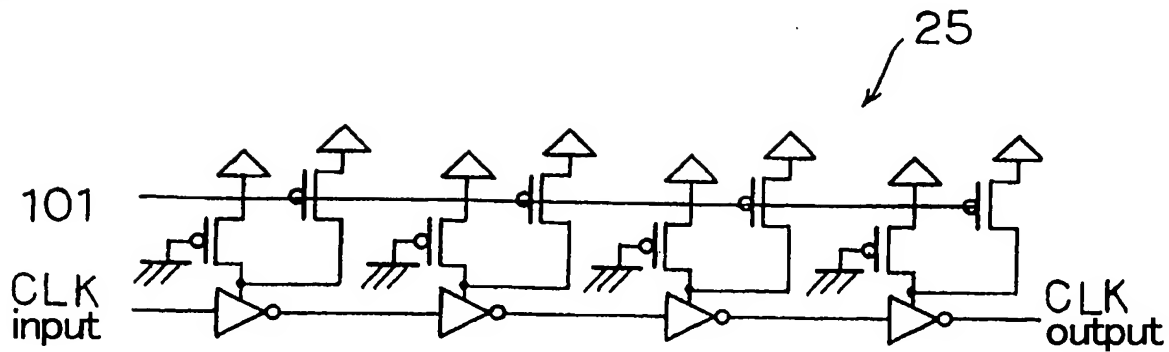


Fig. 46

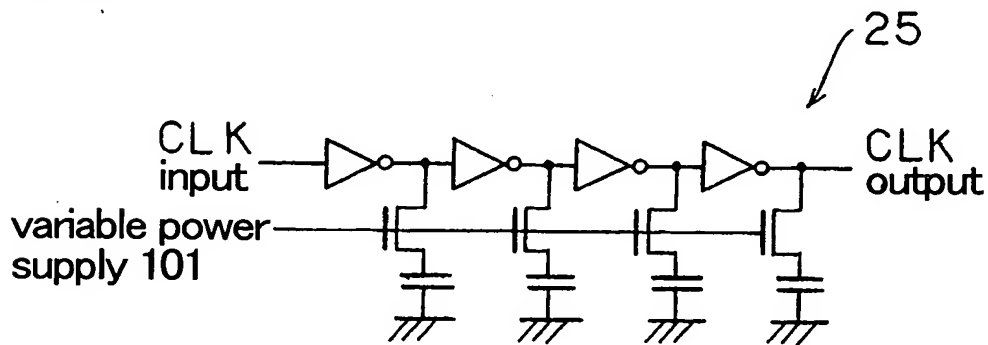


Fig. 47

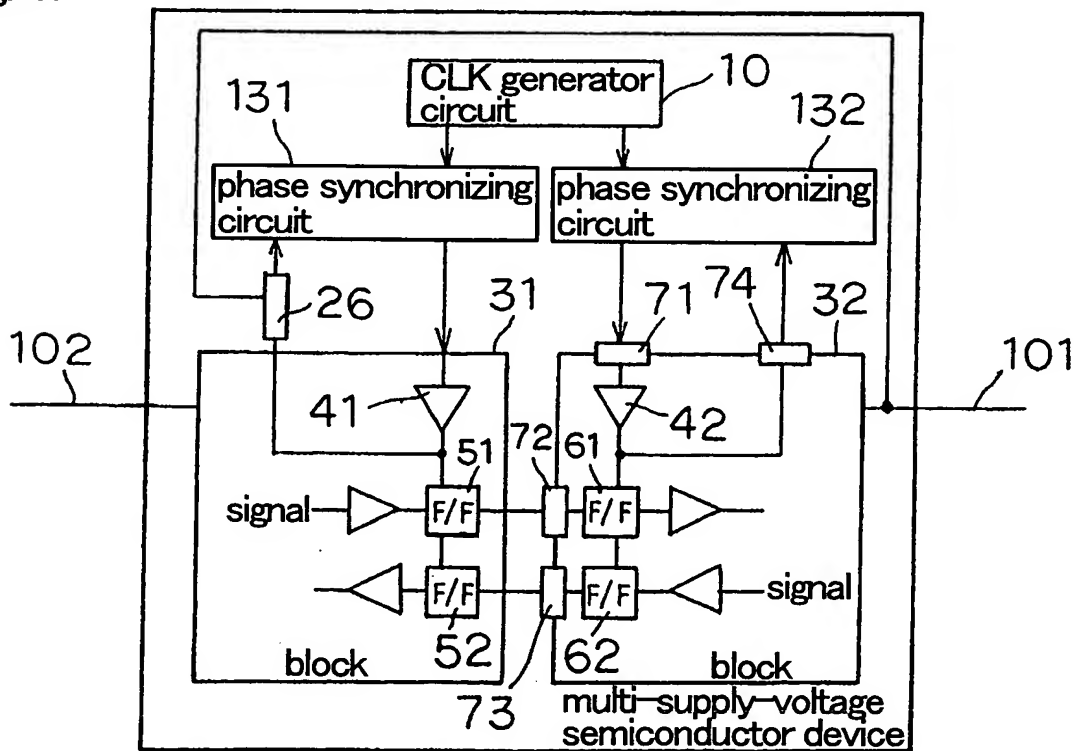


Fig. 48

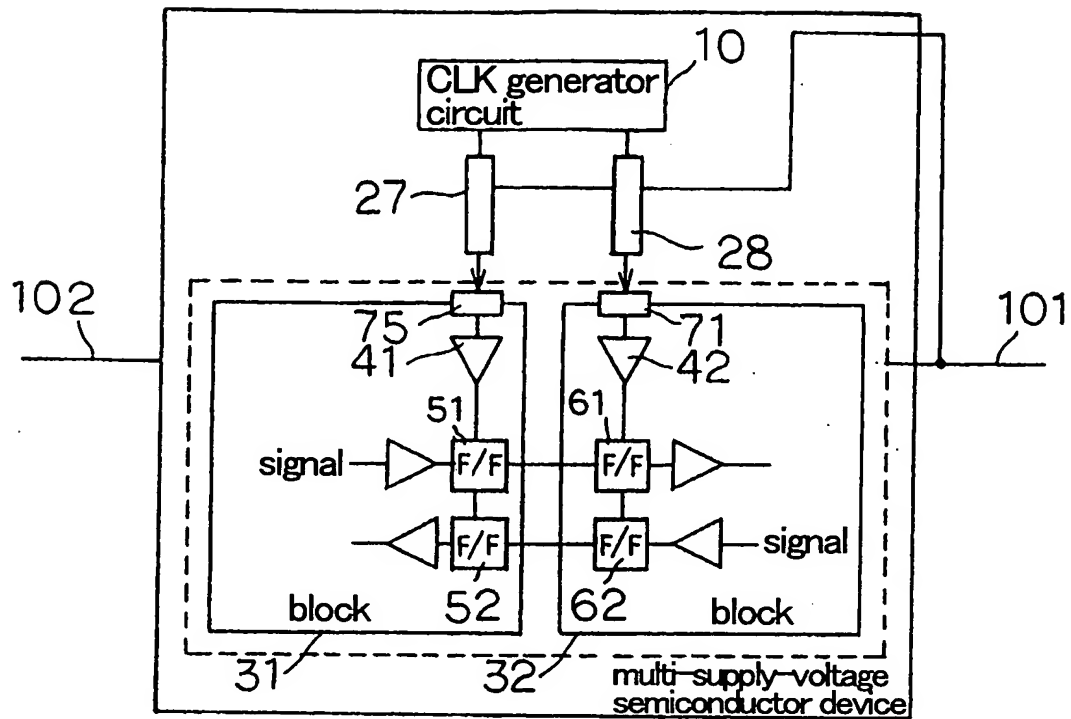


Fig. 49

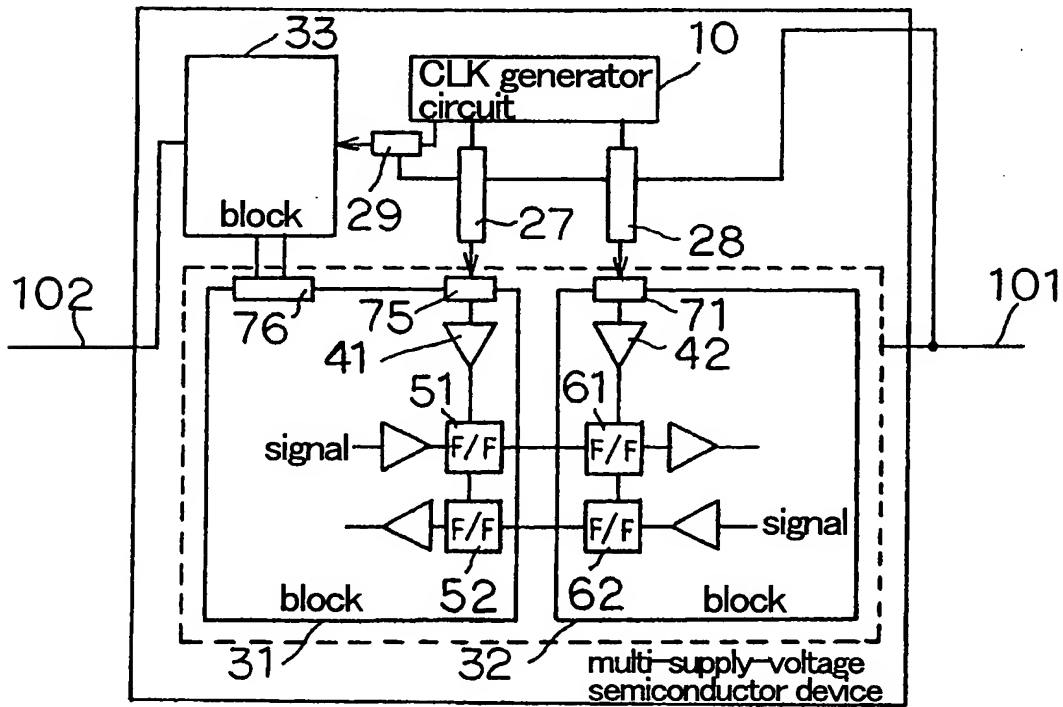


Fig. 50

